

CLAIMS

1. An integrated circuit (IC), comprising:

programmable clock skew logic that applies a
programmed skew amount to edges of a clock signal
selected by a sync signal;

an external interface; and

test logic, coupled to said clock skew logic and to
said external interface, that enables programming
of said programmed skew amount and control of
said sync signal.
2. The IC of claim 1, wherein said test logic executes a
debug routine that programs said clock skew logic and
that controls said sync signal.
3. The IC of claim 1, wherein said test logic enables
access to said clock skew logic by an externally-
coupled chip tester via said external interface for
programming skew and for controlling said sync signal.
4. The IC of claim 1, further comprising:

a clock generator that synchronizes a primary clock
signal with a feedback clock signal;

said clock skew logic including a first clock skew logic block, coupled to said clock generator, that receives a first sync signal and that skews said primary clock signal to provide a skewed primary clock signal;

a clock distribution network that distributes a plurality of duplicates of said skewed primary clock signal on the IC;

a clock phase synchronization node that receives said plurality of duplicates of said skewed primary clock signal and that returns a core clock signal;

said clock skew logic including a second clock skew logic block, coupled to said clock generator, that receives a second sync signal and said core clock signal and that provides said feedback clock signal with compensated skew; and

said test logic providing said first sync signal corresponding to said primary clock signal and said second sync signal corresponding to said core clock signal.

5. The IC of claim 4, wherein said first and second clock skew logic blocks each comprise:

programmable phase adjust logic, coupled to receive a corresponding sync signal being either one of said first and second sync signals, that provides a set of delay bits indicative of said programmed skew amount; and

a clock skew buffer, receiving said set of delay bits and an input clock signal being either one of said primary clock signal and said core clock signal, that delays said input clock signal by an amount determined by said set of delay bits.

6. The IC of claim 5, wherein said phase adjust logic includes a programmable memory for storing a programmed skew value.

7. The IC of claim 5, wherein said clock skew buffer comprises:

a plurality of sequentially-coupled buffers having an input receiving said input clock signal, at least one intermediate node, and an output providing a skewed clock signal; and

at least one array of P-channel and N-channel devices,
each said array having a plurality of inputs
receiving said set of delay bits and at least one
output coupled to said at least one intermediate
node.

8. The IC of claim 7, wherein each of said at least one array of P-channel and N-channel devices comprises an N-channel array including a plurality of binarily-distributed N-channel devices with floating sources having inputs receiving true delay bits from said set of delay bits and having an output coupled to said intermediate node, and a P-channel array including a plurality of binarily-distributed P-channel devices with floating sources having a plurality of inputs receiving complementary delay bits from said set of delay bits and having an output coupled to said intermediate node.
9. The IC of claim 5, wherein said first and second clock skew logic blocks each further comprise:

said set of delay bits comprising a first set of delay bits and said clock skew buffer comprising a first clock skew buffer that receives said first set of delay bits and that provides a first skewed clock signal;

said phase adjust logic providing a second set of delay bits indicative of a default skew value and a select signal controlled by said corresponding sync signal;

a second clock skew buffer, receiving said input clock signal and said second set of delay bits, that delays said input clock signal by a default skew amount determined by said second set of delay bits and that provides a second skewed clock signal; and

select logic having a first input receiving said first skewed clock signal, a second input receiving said second skewed clock signal, a select input receiving said select signal, and an output providing a selected skewed clock signal.

10. The IC of claim 9, wherein:

said phase adjust logic of said first clock skew logic block is programmed with a first skew value; and

said phase adjust logic of said second clock skew logic block is programmed with a second skew value to provide an equal and opposite skew amount of said first skew value relative to said default skew amount.

11. A debug system for varying clock skew of an integrated circuit (IC) for a controllable number of clock cycles, the IC having an external test port, said debug system comprising:

clock control logic integrated on the IC, comprising:

a delay block that delays a selected number of transitions of a first clock signal to provide a second clock signal, wherein each selected transition of said second clock signal is delayed, based on a first sync signal, by either one of a default skew amount and a selected skew amount; and

test logic, coupled to said delay block and accessible via the external test port, that enables dynamic control of said first sync signal and dynamic programming of said selected skew amount; and

a chip tester, coupled to said test logic via the external test port, that provides said selected skew amount and that controls said first sync signal.

12. The debug system of claim 11, wherein said test logic comprises JTAG logic and wherein said external port comprises a JTAG port.
13. The debug system of claim 11, wherein said test logic executes a test routine downloaded from said chip tester that provides said selected skew amount and that controls said first sync signal.
14. The debug system of claim 11, wherein said chip tester executes a test routine that provides said selected skew amount and that controls said first sync signal via said test logic.
15. The debug system of claim 11, wherein said clock control logic further comprises:

a clock generator that synchronizes said first clock signal with a feedback clock signal;

a clock distribution network that distributes at least one third clock signal based on said second clock signal;

a clock phase synchronization node that receives said at least one third clock signal and that returns a core clock signal;

a compensation delay block that delays transitions of said core clock signal corresponding to said selected transitions of said first clock signal to provide said feedback clock signal, wherein each selected transition of said core clock signal is delayed, as determined by a second sync signal, by either one of said default skew amount and a compensated skew amount; and

said test logic providing said first sync signal corresponding to said first clock signal and said second sync signal corresponding to said core clock signal.

16. The system of claim 15, wherein said compensated skew amount is an opposite differential of said selected skew amount relative to said default skew amount.
17. A method of debugging an integrated circuit (IC) by adjusting skew of a primary clock signal for a controllable number of clock cycles, comprising:

providing at least one skew value to the IC;

selecting at least one edge of the primary clock signal; and

delaying a selected number of edges of the primary clock signal according to the at least one skew value.
18. The method of claim 17, further comprising executing a debug routine that provides the at least one skew value and that controls assertion of at least one sync signal to select edges of the primary clock signal.
19. The method of claim 18, further comprising programming on-chip test logic with said debug routine.
20. The method of claim 18, further comprising:

coupling an external chip tester to the IC via a test interface coupled to on-chip test logic; and
said executing a debug routine comprising executing said debug routine on the chip tester to control the IC.

21. The method of claim 17, further comprising:

said delaying a selected number of edges of the primary clock signal comprising advancing or delaying selected edges relative to a default skew amount;

synchronizing the primary clock signal with a feedback clock signal;

distributing a plurality of skewed primary clock signals on the IC to a clock phase synchronization node, which returns a core clock signal; and

compensating skew of edges of the core clock signal corresponding to the selected edges of primary clock signal relative to the default skew amount to provide the feedback clock signal.

22. The method of claim 21, further comprising delaying non-selected edges of the primary clock signal and non-corresponding edges of the core clock signal by the default skew amount.
23. The method of claim 21, wherein said compensating skew of edges of the core clock signal comprises adjusting the edges by an equal and opposite amount relative to the default skew amount.
24. The method of claim 21, further comprising:
- said providing at least one skew value to the IC comprising programming a first skew value and a second skew value on the IC;
- said delaying a selected number of edges of the primary clock signal comprising delaying edges by a skew amount based on the first skew value; and
- said compensating skew comprising delaying edges by a skew amount based on the second skew value.
25. The method of claim 24, wherein said compensating skew comprises phase adjusting the first and second skew values to provide equal and opposite skew amounts relative to the default skew amount.